LINEAR TECHNOLOGY

OCTOBER 1991 VOLUME I NUMBER 2

IN THIS ISSUE . . .

LTC1272: Single-Supply, Sampling 12-Bit ADC Guarantees 3-microsecond Conversions

by William Rempfer

LTC's new 3µs, 12-bit sampling ADC converts 2.5 times faster than any sampling converter offered in the AD7572 pinout. In fact, the LTC1272 converts as fast as the fastest non-sampling AD7572-type ADCs, while providing an on-chip sample-and-hold, single 5V supply operation, and lower power consumption. This article describes the converter's technology, a typical application, some design advantages, and some breadboarding and design techniques.

Technology: High-Speed Design on a Low-Cost Process

The LTC1272 is a high-speed, capacitor-based, sampling A/D converter, designed on a low-cost BiCMOS process. It achieves a 250kHz sample rate and eliminates the need for a fast, external sample-and-hold. The design of the voltage reference and other circuitry allows single 5V supply operation.

A fast-settling DAC design and a new, patented comparator takes the sampling successive approximation (SAR) conversion architecture to new heights in speed. The LTC1272 does so well that it converts faster than many ADCs which use supposedly faster architectures (for example, the 4µs subranging AD678 and AD1678).

In Figure 1, the sample-and-hold function is provided when the input signal is stored on the sample-and-hold capacitor, C_{sample}. The acquisition time to 12 bits is typically 450ns (1µs maximum). Sample-and-hold errors are included in the accuracy specification of the ADC, reducing system errors and cost.

The DAC is a binary-weighted capacitor array that is wafer trimmed to within 1/2 LSB maximum linearity error, using a fusible-link ROM. It is designed to switch and settle extremely quickly. As a result of our attention to process, layout, and design, only the three most-significant bits require trimming.

The comparator is optimized for speed. At a 3µs conversion rate, only 250ns are available for each bit test. To achieve a 3µs spec over temperature

continued on page 8

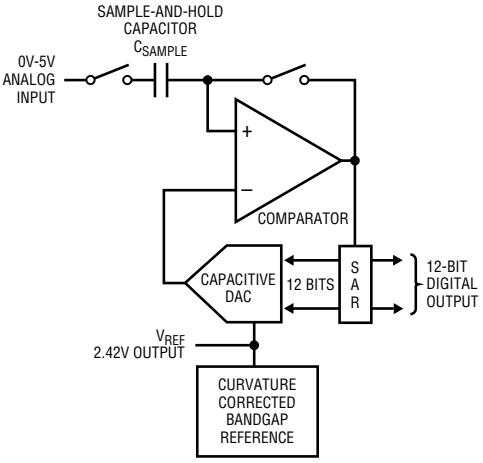

Figure 1. Block Diagram Shows Fast Settling DAC and Patented Comparator: The Heart of the 3µs Sampling ADC

Linear Technology Continues Analog Excellence

by Richard Markell

The second issue of *Linear Technology* from the corporation of the same name, continues to present new products, applications, innovations, and product highlights from the designers at Linear.

Reader response to the first issue of *Linear Technology* has been excellent. Both the overall concept and the technical level of the magazine were favorably received. *LT* will continue to offer both application articles that focus on circuit theory and system design, and articles on the inside details of new products conceived by the designers at LTC.

We would like, in a future issue, to begin a question and answer column driven by reader involvement. If you have a question on a specific circuit problem or an issue that you would like to see addressed in the magazine, please write a note or send a FAX detailing your question to: Richard Markell, *c/o* LTC World Headquarters (see page 20 for our address and FAX number). In addition, do not hesitate to send us ideas and/or suggestions for new products that you would like to see LTC manufacture. *We are always listening!*

Issue Highlights

The second issue of Linear Technology features five "Design Feature" articles. These articles highlight the features and performance characteristics of new LTC products.

William Rempfer, in the first article, introduces the LTC1272, a 12-bit, 3 microsecond, 250kHz sampled-data A to D converter. Willie discusses the technological innovations which allow LTC's first 12-bit parallel A/D converter (with sample-and-hold) to convert faster than any AD7572 type converter. The LTC1272 was first introduced at LTC's popular "For Designers by Designers" seminar series.

John Wright presents the LT1190 series of high-speed, low-cost, video amplifiers in his article. These amplifiers are a significant addition to the LTC product line and are aimed at a wide variety of video as well as general-purpose high-speed amplifier applications. John has been designing integrated circuits for almost fifteen years and high-speed op amps for five of those years. His discussion of the challenges involved in crafting high-speed amplifiers for the bipolar process is quite fascinating, but John is equally capable of discussing fly fishing on Hat Creek with zest.

In his Design Feature, George Erdi discusses the new family of Instrumentation Amplifiers (IAs) recently introduced by LTC. George is the father of the precision low-noise operational amplifiers, having designed such parts as the OP07, the OP27, the LT1028, the LT1013, and the LT1078. George has been with LTC since the company was founded. In his article, George gets right to the heart of the IA issue by offering detailed specifications and selection criteria for each new IA offered by LTC.

Tim Skovmand writes about the LTC1155, a new, low-quiescent-current MOSFET driver designed specifically for low-voltage, high-efficiency switching applications, such as those found in power supplies for notebook and laptop computers. Tim has been designing power control and automotive IC's for almost twelve years and he is a member of the new Power Control Group of designers at LTC.

In our final Design Feature, Rich Markell discusses a filter for data transmission that grew from a customer building the same filter using 29 op amps, 30 adjustments and, in the customer's words, "no cigar." The LTC1264-7 is a linear-phase filter with cut-off frequencies to 200kHz. Rich, in his article, explains the eye-diagram method of filter characterization for data transmission and the uses for this new filter technology.

The "Design Ideas" section presents circuit ideas from Jim Williams on the ultimate in chopper amplifiers as well as an AGC circuit. Steve Pietkiewicz provides a surface-mountable circuit to program Intel memory devices.

The "New Device Cameos" section is presented by LTC Marketing to introduce many new families of devices from LTC. In fact, so many new devices are included in this issue that the "New Device Cameos" page has been expanded to two pages.

HAPPY BIRTHDAY LTC ... and a big thank you to all those who helped establish and run the company during its first ten years. Thanks to all our customers, also!

The LT1190 Family, A Product of Design Innovation

by John Wright

The LT1190 amplifier family is a new series of low-cost, high-speed, video amplifiers from LTC. These amplifiers are aimed at a wide variety of video applications, as well as general-purpose, high-speed amplification. The family consists of three voltage-feedback amplifiers (op amps), and two video-difference amplifiers (video amplifiers with uncommitted (+) and (–) inputs). The performance levels attained with these amplifiers have traditionally been realized only with more expensive processes, such as full-complementary or dielectrically isolated technologies. The LT1190 family is unique because of its patent-pending circuitry, and because it is fabricated on a low-cost bipolar process with high-speed NPN and slow lateral PNP transistors.

All of the LT1190 series amplifiers drive video cables directly at 450V/µs, they source and sink 50mA of output current, and have gain-bandwidth products ranging from 50 to 350MHz. The family is optimized for ±5V supplies, and is guaranteed from ±8V down to a single +5V supply.

The Challenges of High Speed

The lateral PNP transistors of standard bipolar IC processes cause problems in all but general-purpose, low-frequency amplifiers. They are much slower than NPNs, and have f_ts less than 10MHz, greatly limiting their usefulness in fast amplifiers. While they are suited for level shifters at DC, they are unacceptable for fast AC signals due to excessive phase shift.

The classic solution to this problem is to pass AC signals around the PNPs by means of a *feedforward* capacitor, as used in amplifiers such as the LM118. However, this technique causes serious settling-time problems, with "long tails" of up to several microseconds. Other response anomalies must also be well controlled. For clean settling dynamics, the net open-loop response of an amplifier should closely resemble a single-pole roll-off, a difficult goal to achieve as bandwidth increases and multiple poles and zeros contribute phase shift. The poor settling time often associated with feedforward amplifiers is due to doublets, or closely-spaced pole zero/pairs in the signal path. Indeed, examination of the 118's rolloff shows just such a doublet "bump." In the design of the LT1190 series amplifiers, several design innovations contribute to a well controlled gain/phase response, resulting in good settling characteristics.

What's Inside?

Figure 1 is a schematic of the LT1190/91/92 op amps, revealing how the settling-time problem was addressed via several design steps. The NPN input stage has a single-ended output taken from the collector of Q1, instead of a differential output as in other designs. This measure eliminates the shunt capacitor otherwise needed on the collector of Q2 (used to produce single-ended AC level shift drive). In such shunt-capacitor-based designs (e.g., the 118) settling time is degraded by the input stage, which generates a pole/zero pair separated by an octave.

In the second stage of LT1190 circuit, a local DC reference voltage V_{ref} is generated, which tracks Q1's collector. This feature provides the amplifier with a low V_{os}, just as if a more conventional differentially loaded Q1–Q2 stage were used.

The second stage of the amplifier, consisting of Q3 through Q8 and their associated components, functions as a DC-balanced, AC-feedforward level shifter. The transconductance of the level shift is set by R2, R3, Q5, and Q6, while C_{FF} feeds AC signals around Q6. A second doublet is formed by the f_t of PNP Q6 and feedforward capacitor C_{FF}. However, by enclosing the level shifter within the Q9–Q10 integrator loop, the effects of this doublet are reduced as a result of Q10's gain. Also, unlike previous designs, there is no AC signal path through the current mirror Q7–Q8, which could otherwise cause high-frequency phase shift in the level shift.

In keeping with a single-ended design, the output stage is a class-AB

continued on page 11

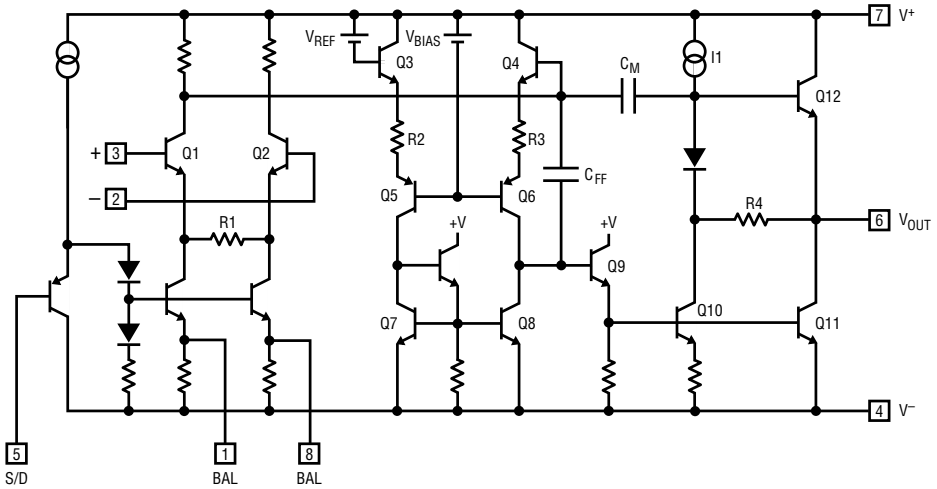

Figure 1. LT1190 Family Low Cost Operational Amplifier

New LTC1264-7 Allows Linear Phase Data Transmission to 200kHz

by Richard Markell

Introduction

The pace of digital communications is increasing at a tremendous rate. Daily, the digital data-compaction engineer is expected to transmit more data in the same channel bandwidth with closer channel spacing. All known compaction techniques involve simultaneous combinations of amplitude and phase modulation to reduce the bandwidth-to-data-rate ratio. Filter design has not kept up with this "compact-or-else" scenario until now. Although filters such as the LTC1064-3 linear-phase, switched-capacitor filter have excellent transient response, they have poor adjacent-channel rejection. DSP is a help if the designer is working with telephone bandwidths, but it is not fast enough for efficient use of 100kHz of bandwidth, let alone 200kHz, where one can send 400–800kbits/second of data.

Non-Bessel linear-phase filters and other non-traditional filter designs were difficult to implement before the development of the FilterCAD design software, and, as a result, such designs were seldom employed. Expensive test procedures, network analyzers, and difficult adjustments are required for the successful implementation of these filters. With the aid of FilterCAD, LTC has created the LTC1264-7 linear-phase filter, thus sparing digital communications engineers from the challenges of non-traditional filter design.

Although its group delay is equal to that of the Bessel in the pass band, the LTC1264-7 has stopband rejection at the second harmonic of the cut-off frequency of –30 dB, versus the Bessel's –12dB. Even the most conservative data-compaction engineer will agree that the LTC1264-7 is "better than Bessel." Enough hoopla—let's get into the details.

For the first time in history, Linear Technology has incorporated two complex poles and two complex zeros of phase compensation and six real poles plus two real zeros of low-pass elliptic filtering into a single 14-pin package. This is the LTC1264-7 filter. Just decide on a cutoff frequency and specify the appropriate clock frequency. No external resistors are required. The LTC1264-7 is the first member of the linear phase filter family: the "-7s." This group will include, in addition to the LTC1264-7, the low power (4mA) LTC1164-7, with cutoff frequencies to 20kHz, and the originator of the family, the LTC1064-7, which will provide cutoff frequencies to 100kHz.

The eye diagram shown in Figure 1 illustrates 100 kHz phase performance. Notice the lack of overshoot or undershoot at the transitions. The real advantage of the LTC1264-7, however, is in its stopband rejection. Figure 2 shows an amplitude comparison of the responses of the LTC1264-7, the 8-pole Butterworth (the LTC1064-2), and the 8-pole Bessel filter (the LTC1064-3). The difference is dramatic. The LTC1264-7 attains 30dB attenuation at two times cutoff, while the LTC1064-3 attains only 12dB. The phase responses of both filters remain linear through their passbands, although the LTC1064-3 extends this response to almost two times cutoff. We will explore the effect this has on digital transmission later in this article, but to make this comparison, a short explanation of some principles of digital transmission is first needed.

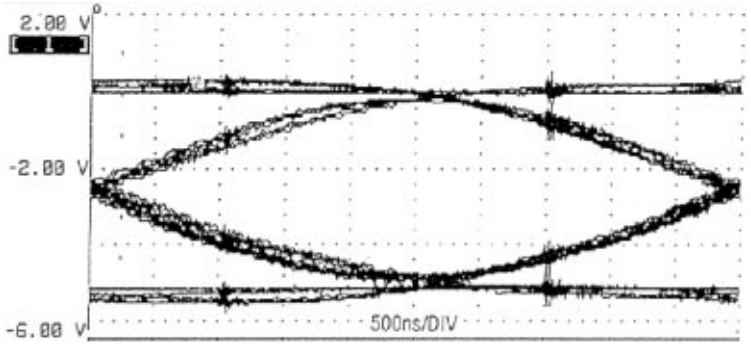

Figure 1. LTC1264-7: f_{CUTOFF} = 100kHz, f_S = 200kb/s. ISI Degradiation = –1.2dB, Peak Jitter = 600ns (Not Measured in This View)

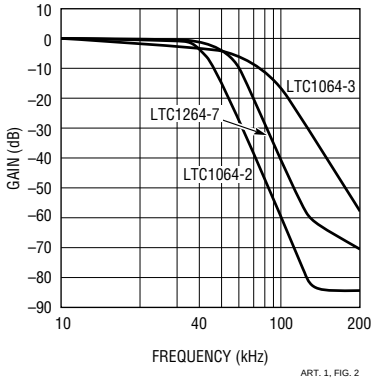

Figure 2. Filter Roll-Off Comparison, f_{CUTOFF} = 40kHz, for Butterworth 8th Order Lowpass Filter (LPF), LTC1064-2, Bessel 8th Order LPF, LTC1064-3, and LTC1264-7 Linear Phase Filter

Some Principles of Data Transmission

Transmission of data in a channel with a given bandwidth is most efficient when as many bits-per-second as possible can be transmitted through said channel. Nyquist theorems show that the theoretical data-rate limit is

continued on page 13

The LTC1100, LT1101 and LT1102: A Trio of Effective Instrumentation Amplifiers

by George Erdi

Next to the universally used op amp, perhaps the most useful linear-IC building block is the instrumentation amp, or "IA." Using IA's effectively can in some ways be more challenging than selecting op amps, because IA's have different specs, and can also use different topologies. However, the basic task is a fixed-gain, differential-input, single-ended output amplifier, the definition of an IA. The differential signal typically rides on top of a common-mode signal; the differential input is amplified and the common-mode voltage is rejected by the IA.

The instrumentation amplifier can be implemented with dedicated IA designs, or with one to three op amps to realize the gain function, and a minimum of four ratio-matched precision resistors, configured as two like-ratio pairs.

The most familiar IA type is the single-op-amp variety, usually called a difference amplifier, and shown in Figure 1a. Using just two parts (one op amp and one resistor network), this IA is the height of simplicity and utility. For modest requirements, it is built with just a general-purpose op amp and four precision resistors. A drawback to this type of IA is that the resistor bridge loads the source. The three-op-amp configuration uses seven resistors and has high input impedance. It is obviously more difficult to implement than the single-op-amp version. A nice compromise between these two approaches is illustrated in Figure 1b. This IA design uses two op amps to buffer the signal inputs and requires only four resistors. The use of two op amps with modern dual devices causes no penalty, and in fact this arrangement has real virtues over the more basic setup of Figure 1a.

This IA architecture presents minimum loading to the differential source, namely the bias current of the op amp used, which is balanced between the two inputs. The resistor network needs very precise trimming for high common-mode rejection (CMRR) and gain accuracy. The trimming is non-interactive; first the R4/R3 ratio is trimmed for gain accuracy, then the R1/R2 ratio is trimmed for high CMRR. Trimming compensates not only for resistor inaccuracies, but also for the finite gain and CMRR of the op amps. The amplified difference appears between the output terminal and the voltage applied to the REF terminal (normally grounded).

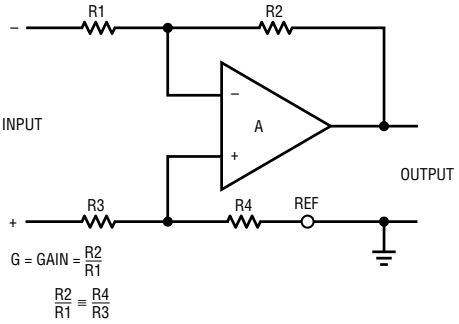

Figure 1a. Basic Single Op Amp Instrumentation Amplifier

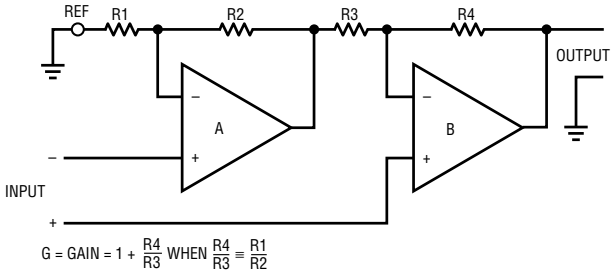

Figure 1b. Buffered Dual Op Amp Instrumentation Amplifier

As a basic building block, this IA can be performance optimized for various applications by a choice of op amps. LTC has taken this step with the LTC1100, LT1101, and LT1102, an instrumentation-amplifier series offered in an 8-pin footprint with connections as shown in Figure 2. As illustrated, the gain of these IA's is user programmed by taps on the resistor array, for pre-trimmed precision gains of either 10 or 100 for the LT1101

continued on page 14

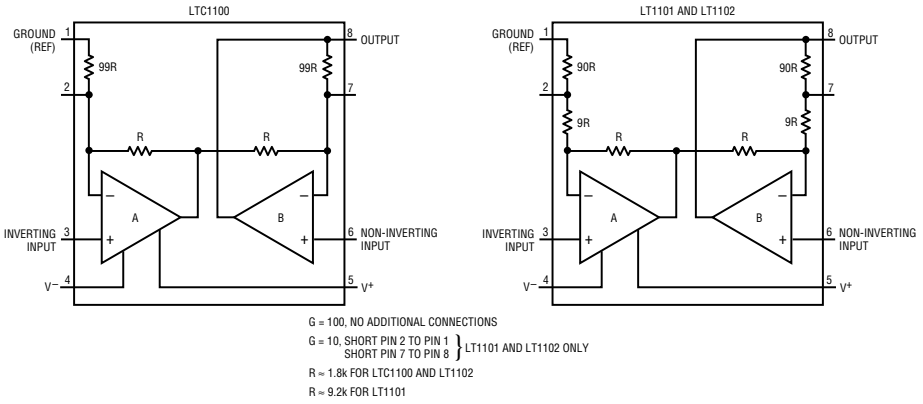

Figure 2. Instrumentation Amplifiers in 8-Pin Packages

The LTC1155 Dual, High-Side MOSFET Driver

by Tim Skovmand

The LTC1155 is a new, micropower MOSFET driver, specifically designed for low-voltage, high-efficiency switching applications, such as those found in lap-top or notebook computers. The LTC1155 facilitates the use of low cost, N-channel MOSFETs in place of the larger and more expensive P-channel devices used in many applications.

The LTC1155 does this by producing a gate voltage higher than the power supply rail. This higher voltage is produced by on-chip capacitors which successively deliver charge to the gate of the power MOSFET. This so-called "charge pump" has been designed to be very efficient, requiring only 8µA in standby mode and 85µA in operation from a 5 volt rail while producing 7 volts of gate drive (12 volts above ground). This efficiency is due in large part to the capabilities afforded by the proprietary LTC CMOS process, which yields low-leakage, compact capacitor structures and efficient CMOS switches.

The LTC1155 also includes two independently operating protection circuits. These circuits are designed to detect a drop of 100mV across a sense resistor in series with the drain of the power MOSFET. If this limit is exceeded, the gate of the MOSFET is quickly discharged (pulled to ground) and the MOSFET protected against destructive over-current conditions. A delay can be inserted between the sense resistor and the drain sense input in order to prevent false triggering while driving high inrush loads, such as large capacitors, DC motors, or lamp loads.

The LTC1155 is a true, mixed analog and digital system, as evidenced by the block diagram shown in Figure 1. The block diagram reveals the careful segregation of analog and digital functions.

The analog section, containing the 100mV reference, comparator, and an internal 10µs delay, is powered from a separate voltage regulator to eliminate the possibility of interference or false triggering by the densely packed CMOS logic section. The analog reference and comparator devices are relatively large compared to their digital counterparts, so as to reduce offsets and increase gain.

APPLICATIONS

Lap-top Computer Power Management

Lap-top computer power must be managed very carefully because the battery pack is a finite energy source. Low loss (efficient) switching is required to gain the maximum operating time from the discharging batteries.

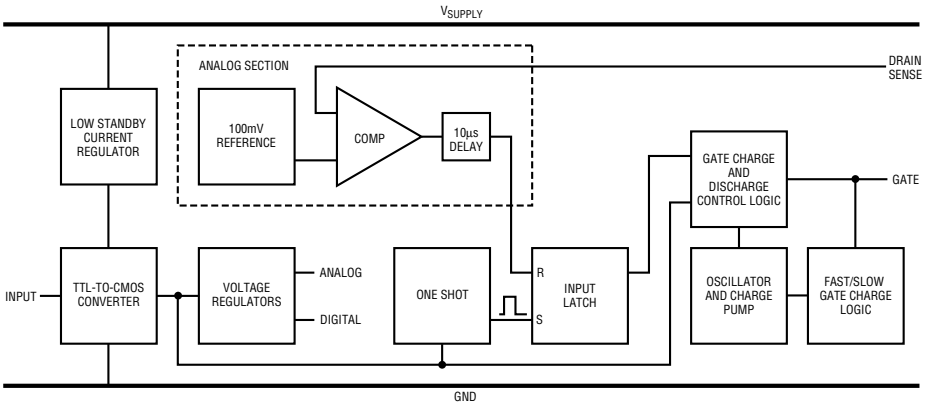

Figure 1. LTC1155 Block Diagram

The digital portions of the LTC1155 are designed for maximum packing density and are therefore powered from a low-voltage regulator. The inputs and outputs to these sections are interfaced by level-shift circuitry, which translates the input TTL levels to CMOS levels and converts the low-voltage CMOS levels back to the rail-to-rail levels used by the gate charge and protection circuitry.

The ultra-low standby current, typically 8µA, is achieved by removing power from all the analog and digital circuit blocks when the input is turned off. Only the two TTL-to-CMOS converters are continuously powered. The gate of the MOSFET is held low via a high-voltage, N-channel CMOS switch that is voltage driven and therefore requires no power.

The LTC1155 facilitates the use of extremely low loss, N-channel MOSFET switches to control the flow of energy to the variety of loads found in a computer system.

Figure 2 is a schematic diagram that demonstrates the use of the LTC1155 for switching the power buses in a lap-top computer system. The disk drive, display, printer and the microprocessor system itself are selectively engaged via high-side switching with minimum loss and are shutdown completely when not in use.

The quiescent current of the LTC1155 is designed to be extremely low in both the OFF and ON states, so that efficiency is preserved even when driving loads which require very little

continued on page 7

LTC1155 continued from page 6

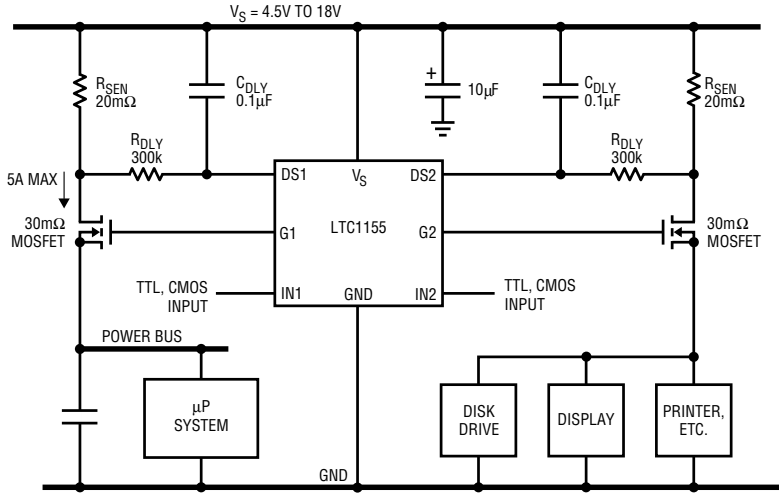

Figure 2. Laptop Computer Power Bus Switching

current to operate in standby, but require much larger peak currents when in operation. This combination of a low RDSon MOSFET and an efficient driver delivers the maximum energy to the load.

Protected SCSI Termination Power

The circuit shown in Figure 3 demonstrates how the LTC1155 provides protected power to SCSI terminators. The LTC1155 is initially triggered by the free-running 1Hz oscillator (it could also be triggered by a pulse from the microprocessor) and latches ON via the positive feedback provided by R_{fbk}. The power MOSFET gate is driven to 12V and the MOSFET is fully enhanced.

The delay afforded by the two delay components, R_{dly} and C_{dly}, ensure that the protection circuit is not triggered by a high inrush-current load. If, however, the source of the MOSFET is shorted to ground, or if the output of LT1117 is shorted, the delay will be exceeded and the MOSFET will be held OFF until the pulse from the free-running oscillator resets the input again. The drain sense resistor, R_{sen}, is selected to trip the LTC1155 protection circuitry when the MOSFET current exceeds 1A. This current limit protects both the LT1117 and any peripheral system powered by the SCSI termination power line.

The delay time afforded by R_{dly} and C_{dly} is chosen to be considerably smaller than the reset time period (>100:1), so that very little power is dissipated while the short circuit condition persists, i.e., the LTC1155 will deliver small pulses of current during every reset time period until the short circuit condition is removed.

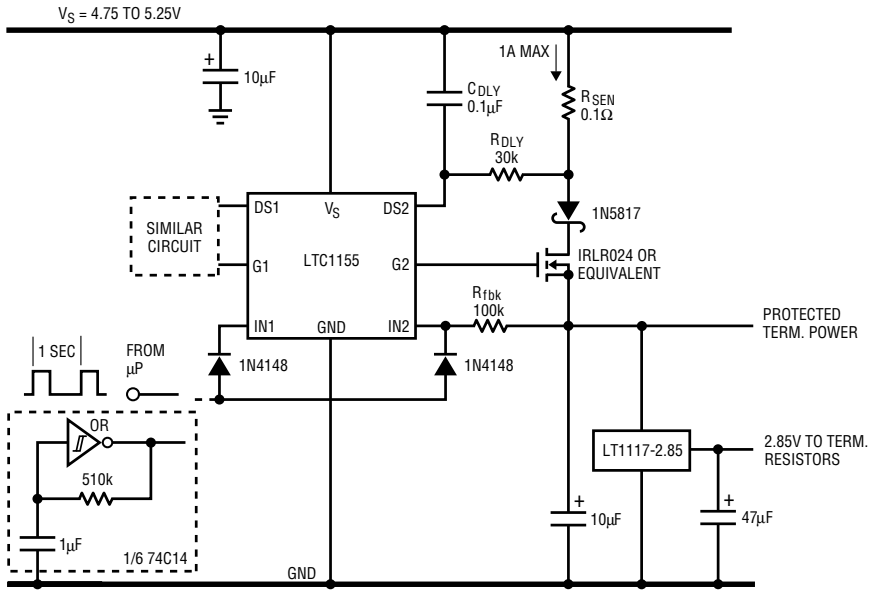

Figure 3. SCSI Termination Power with Short Circuit Protection

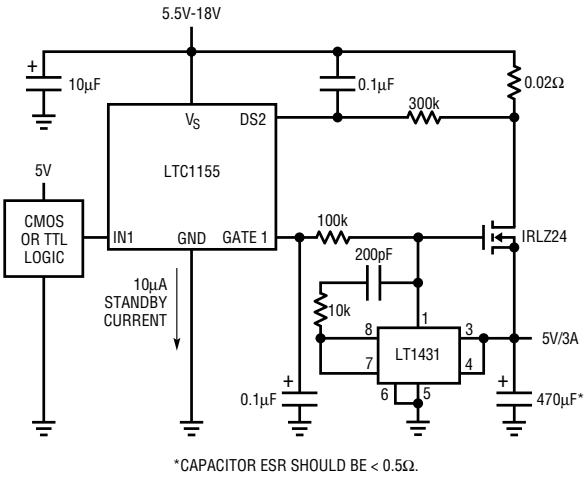

Figure 4. 5V/3A Extremely Low Voltage Drop Regulator

The LTC1155 and the LT1117, as well as the power MOSFET shown, are available in surface mount packaging and therefore consume very little board space.

Extremely Low Voltage Drop Regulator

An extremely low voltage drop regulator can be built around the LTC1155 and a low-resistance power MOSFET, as shown in Figure 4. The LTC1155 charge pump boosts the gate voltage above the supply rail and continuously charges a 0.1µF reservoir capacitor. The LT1431 works against this capacitor and the 100k series resistor to

continued on page 15

LTC1272 continued from page 1

and process extremes, the typical conversion time must be about 2µs, or 170ns per bit test. In that time, the DAC must settle, the comparator must make a bit decision, and the successive approximation register (SAR) must latch the bit value and update the DAC. The SAR consumes roughly 30ns, which leaves 140ns for the DAC and the comparator. The speed was achieved by means of a DAC which settles to 0.002% in 80ns and a high-gain, wide-bandwidth comparator, which responds in 60ns to an overdrive of 30µV. The comparator is oscillation free, in spite of its gain-bandwidth product of 60GHz (2k • 30MHz bandwidth). The comparator is also designed to cause minimum disturbance to the power supply and ground lines. This makes the ADC remarkably easy to use, considering its speed.

The curvature-corrected bandgap reference provides 25ppm/°C maximum full-scale drift on a single 5V supply. (We chose a bandgap reference because 5V is not enough to power a buried-zener reference.) The reference-output voltage is nominally 2.42V. (This differs from the –5.25V reference voltage of the AD7572, but the LTC1272 design provides the same 0V to 5V input range as the AD7572. It is plug-compatible with the AD7572 if the polarity of the bypass cap is reversed.)

A Typical Application: 12 Bits on a Single 5V Supply

The typical hookup in Figure 2 shows a single 5V system that can convert 0-to-5V input signals at a 250kHz rate. A single-point "star" ground is formed to the analog ground plane at the LTC1272 analog ground pin. The power-supply and reference-output pins are each bypassed to the analog ground plane with a 10µF tantalum in parallel with a 0.1µF disk ceramic. Pin 23 is not internally connected and can accommodate the –15V supply of the AD7572 and its copies. The digital ground pin is also tied to the analog ground plane.

The analog input range is 0V to 5V. The conversion time is set by the frequency of the clock applied to the clock-input pin, CLK_{IN}, (4MHz for 3µs conversion time). The conversion is started and read with the chip select ($\overline{CS}$), read ($\overline{RD}$), and high-byte-enable (HBEN) inputs and the end of the conversion is detected with the $\overline{BUSY}$ output. Data can be read as either a 12-bit word or two 8-bit bytes on the data outputs (D0/8-D11).

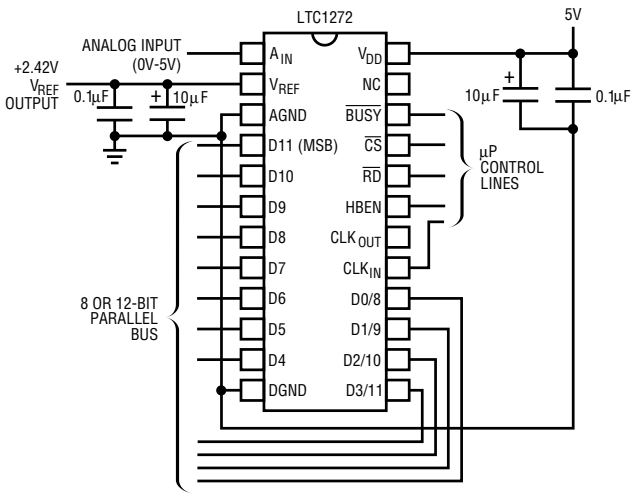

Figure 2. 12-Bit, Single 5V System Converts AC or DC Inputs

Design Advantages: System Performance and Cost

Both DC and AC signals can be digitized. DC performance is shown by Figure 3, a curve of typical integral nonlinearity (INL) and differential non-linearity (DNL). DC specs include ±1/2 LSB INL over temperature. 12-bit, no-missing-code resolution is assured by ±1 LSB DNL. The conversion time is 3µs, which is faster than the non-sampling 5µs AD7572 and equal to the

continued on page 9

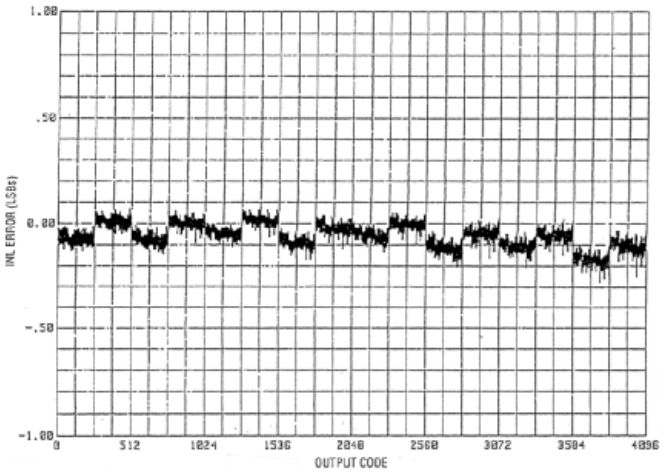

Figure 3a.

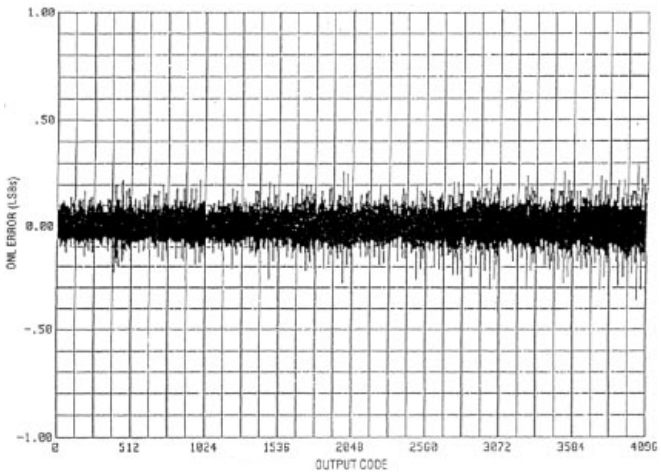

Figure 3b.

Figure 3. DC Performance is Typically Much Better Than the Specifications of a) ±0.5 LSB Maximum INL, and b) ±1.0 LSB Maximum DNL

LTC1272 continued from page 8

fastest AD7572 copy. Full-scale error is ±10 LSBs, with a maximum temperature drift of 25ppm/°C. Maximum power consumption is 100mW, 45% less than that of the AD7572.

Time-domain AC performance is characterized by the 1µs maximum 0.01% acquisition time of the sample-and-hold. In SAR ADCs without sample-and-holds (e.g., the AD7572), signal bandwidths must be restricted to avoid conversion errors, often to frequencies below 10Hz. Also, the buffer driving the analog input must have extremely low output impedance at high frequencies in order to hold the analog input stable in the presence of large input-current transients that occur during the conversion. In contrast, the sampling LTC1272 can handle rapidly changing inputs and does not require the complex input buffer.

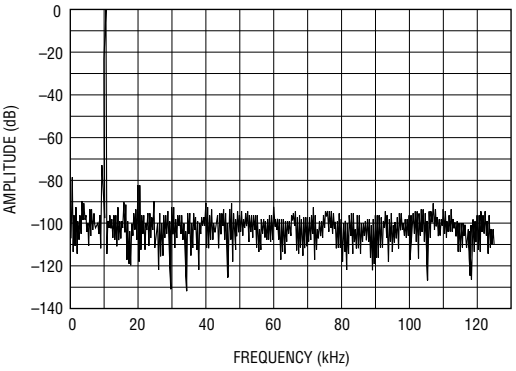

Figure 4. AC Performance is Characterized by the FFT of the Output Spectrum. S/(N + D) = 71.6dB, Effective Number of Bits (ENOBs) = 11.6

Figure 4 shows an FFT plot taken at a sample rate of 250kHz and an input signal of 10kHz. Signal to noise plus distortion (S/(N+D)) is 71.6dB.

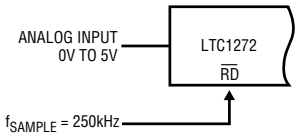

Figure 5a.

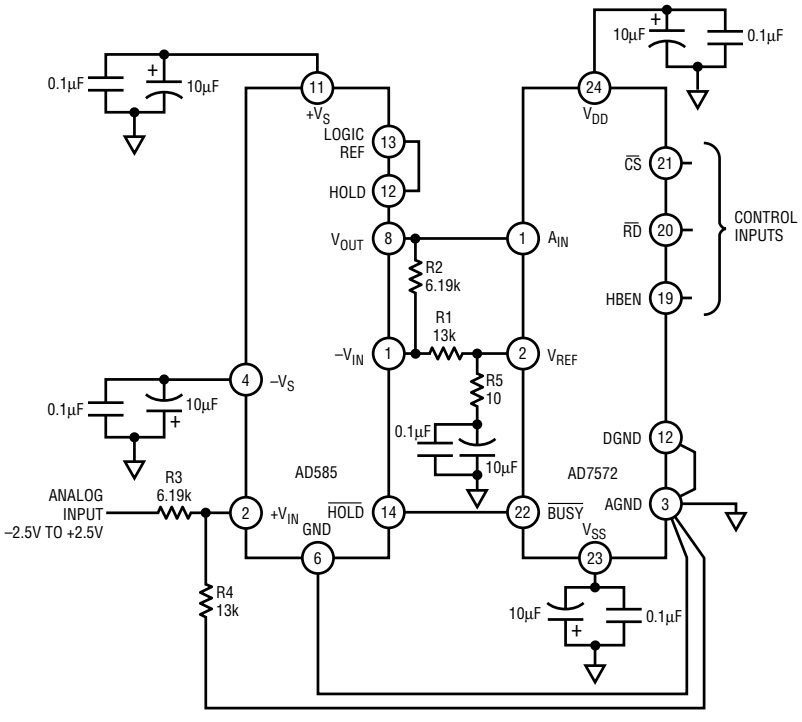

Figure 5b.

Figure 5. For Sampling Systems, the Sampling LTC1272 a) Offers Cost, Power, Speed, Accuracy and Board Space Advantages over the Non-Sampling AD7572 with an External Sample-and-Hold, b). The LTC1272 Sample-and-Hold is Invisible to Users Who do not Require It

Cost-effective system design results from the LTC1272's features. Providing the sample-and-hold at the same conversion speed saves cost and board space, reduces power consumption, and improves accuracy (see Figure 5). Single-supply operation can also save power and eliminates the need for a negative supply (see Figure 6).

Breadboarding and Design: Four "Inputs" to any ADC

To breadboard and design with ADCs it helps to recognize that any ADC has at least four inputs (see Figure 7):

1. The analog ground pin, AGND
2. The analog input, A_{IN}
3. The reference, V_{REF}
4. The power supplies (in this case only one supply: V_{DD})

To achieve high accuracy and low noise, system design should concentrate on eliminating noise on these four "input" pins.

If a well-designed and correctly functioning ADC gives erroneous output codes, it is doing so for a reason. These erroneous outputs can be DC errors, noisy codes, or tones and harmonics in the frequency domain. If you're not getting the answer you expect, it is probably because some unexpected

continued on page 10

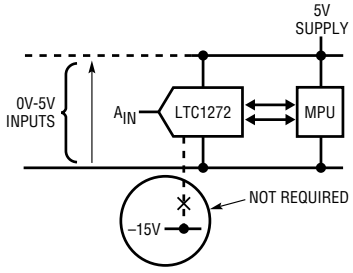

Figure 6. The –15V Supply of the AD7572 is not Required for the LTC1272 Converter Making Single 5V Supply Applications Possible. Because the LTC1272 has an Unconnected Pin Where the AD7572's –15V Supply is, It can Upgrade AD7572 Designs without Board Changes

LTC1272 continued from page 9

condition exists on one of the four inputs. If you know the pin conditions, then the answer the ADC is giving will make sense.

The task in troubleshooting ADC systems is to find out which of the four inputs has something unexpected on it. Then make circuit changes to restore that pin to the desired condition. It's that simple.

The task in designing ADC systems is similar: take steps ahead of time in the design and layout to ensure that pin conditions will be as desired. The steps shown in Figure 7 help ensure proper conditions on the four pins:

A single-point ground should be formed by constructing an analog ground plane around pin 3 (AGND) of the LTC1272. This becomes the zero reference for all analog circuitry. Noise on this ground adds directly to the analog input. Pin 12 (DGND) of the LTC1272 should also be connected to the ground plane. This ground plane should have only one connection to the rest of the system ground. This prevents system-ground currents from taking a short cut through the analog ground. This single connection should be made to a point on the ground plane near the DGND pin.

The circuitry driving the analog input, A_{IN}, must be referenced to the single-point ground near pin 3 of the ADC. The analog signals should be routed away from all digital circuitry. It is also a good idea to shield the analog signal lines with analog ground wherever possible. Shielding digital signal lines with digital ground also helps reduce the magnetic radiation of the digital currents by keeping the loop area of the digital return currents small (see Figure 8). For best analog performance, the input clock (CLK_{IN}) should be synchronous with the $\overline{CS}$ and $\overline{RD}$-conversion start signals (for example, derive the CLK_{IN} signal from the processor clock). This keeps digital-clock noise from coupling into the input when the sample-and-hold goes into hold mode.

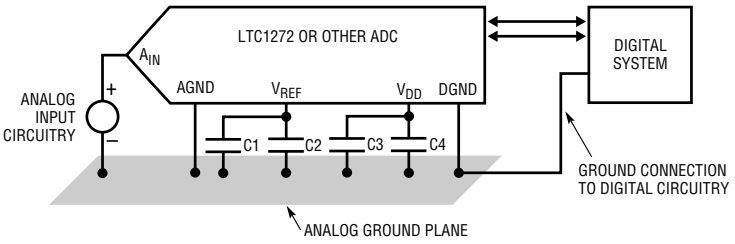

Figure 7. Noise on All Four of the Potential "Inputs" of an ADC Must be Minimized by Referencing Them to a Single Point Ground Plane

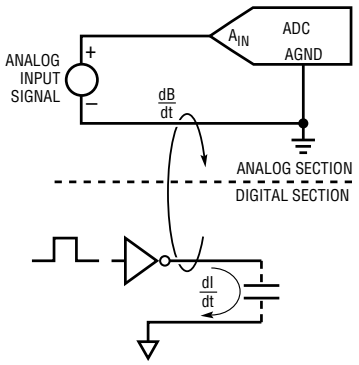

Figure 8. Digital Signals can Couple Magnetically to Analog Sections Through What is Effectively an Air Transformer. To Reduce This: 1) Separate Digital and Analog Sections as Much as Possible, and 2) Reduce the Area of Both Loops by Putting Analog Ground Plane Under Analog Signals and Digital Ground Under Digital Lines

Noise on the voltage reference has a unique signature: it contributes no noise at zero-scale inputs but adds to the converter noise increasingly as the ADC output moves from zero scale to full scale. To minimize reference noise, bypass the reference directly to the analog ground plane with a 10µF tantalum paralleled by a 0.1µF ceramic with short leads (C1 and C2 of Figure 7).

Noise on the power supply can also cause ADC errors. At low frequencies, the converter has very good power-supply rejection, but as the frequency increases, all converters lose the ability to reject power supply noise. Unfrotunately most power-supply noise is high frequency noise, so bypassing to eliminate it is critical. To eliminate power-supply noise, the V_{DD} pin should be bypassed directly to the analog ground plane with a 10µF tantalum in parallel with a 0.1µF ceramic with short leads (C3 and C4 of Figure 7).

Conclusion

With the LTC1272, you can get a 2.5 times speed increase in designs which use other companies sampling AD7572 clones. You can also upgrade your standard, non-sampling AD7572 designs or get 3µsec, single supply, sampling 12-bit conversion in your new designs.

For further information refer to the LTC1272 data sheet and upcoming Application Notes and Design Notes.

LT1190 Family continued from page 3

emitter follower, with a 10mA quiescent current and the ability to slew a 20pF load at over 450V/µs. The stage also has an intrinsically low output impedance, about 2.5Ω open-loop at low frequencies. For sinking more than 10mA in the output stage, extra drive current is supplied to Q11, from R4 and Q10.

In addition, the LT1190/91/92/93 include an optional logic-controlled shutdown feature. With pin 5 open, these devices operate in their normal mode. However, when this pin is pulled to the V– potential, the supply current drops to 1.3mA, and the output is forced into a high impedance state. The outputs of these amplifiers can then be WIRE-OR connected, and selected with low cost logic for multiplexing video signals to a cable.

As with all amplifiers, LT1190 series power supply rejection degrades at high frequency. To achieve minimum settling time, multiple low ESR/low inductance bypass capacitors should be used, such as 0.1µF ceramic discs paralleled by 4.7µF tantalums. In addition, compact layout and ground-plane construction with appropriate high-frequency techniques should be used for best results. When pushing for maximum bandwidth with the op amps, it also helps to use low feedback impedances for R_f and R_g, say, 300Ω, which reduces the effects of stray capacitance on the (–) input.

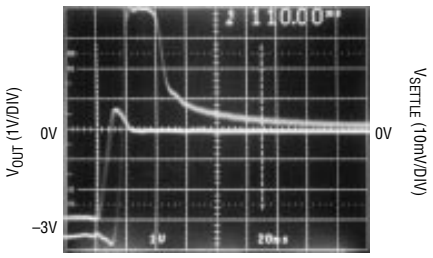

Figure 2: LT1191 settling from a 3V step. A_V = –1

The single-ended output design and the overall attention to open-loop doublets results in very clean settling, as shown in Figure 2. For this test, an LT1191 is operated in a gain of –1, the input step is from +3V to 0V, and settling time to 0.1% is within 110ns. The observed output settling is not a false sum node, but rather the true output.

LT1190 Family Members

A specification summary of the entire LT1190 family is detailed in Table 1. Of the three op amps, the 50MHz unity-gain-stable LT1190 is most tolerant of power-supply bypassing and capacitive loading, but has slightly less gain and more DC offset than the LT1191. The higher gain and lower offset 90MHz LT1191 is also unity-gain stable, and produces only 0.1% differential gain and 0.06 degrees of differential phase shift in 3.58MHz NTSC video use. For applications with a minimum gain of +5, the 350MHz LT1192 operates with even lower errors, and is well suited for high-gain applications such as photo-diode amplifiers.

Comparison of the LT1193 and LT1194 video difference amplifiers is not adequately covered by the table, as they have a unique functional topology that is unlike that of the op amps. These ICs have two uncommitted, high-input-impedance differential inputs, both (+) and (–), and a CMRR in excess of 40dB at 10MHz. They function in either single-ended or differential configurations, making them ideal for video loop-through connections. The LT1193 has adjustable gain set via two external resistors for $A_V \geq 2$, whereas the LT1194 has an internally fixed gain of ±10.

Although the LT1193/94 video amplifiers are similar in some respects to the op amp family members, there are some clear differences, as shown in Figure 3. To make a video difference amplifier, another differential input stage, consisting of Q3 and Q4, was added to the LT1190 op amp, as shown in the figure. This differential amplifier acts as a reference and feedback connection, freeing Q1 and Q2 to serve as the uncommitted differential inputs.

In the LT1193, the feedback resistors are *external*, giving two sets of (+) and (–) inputs for signal input and gain adjustment/DC control, pin pairs 2-3 and 1-8, respectively (plus the aforementioned shutdown option, at pin 5).

In the LT1194, the feedback resistors are *internal*, for a fixed gain of 10,

continued on page 12

Table 1. Typical LT1190 Family Performance

	Op Amps		Video Difference Amps		
	LT1190	**LT1191**	**LT1192**	**LT1193**	**LT1194**
Input V_{os} (mV)	2.0	1.0	0.2	2.0	1.0
Input I_B (mA)	0.5	0.5	0.5	0.5	0.5
CMRR (dB)	70	75	90	80	90
A_{vol} (V/mV, RL=1kΩ)	22	45	225	25	NA
V_{out} (V)	±4	±4	±4	±4	±4
I_{out} (mA, min)	±50	±50	±50	±50	±50
Slew Rate (V/µs)	±450	±450	±450	±450	±450
GBW (MHz)	50	90	350	70	35 (–3dB)
Min Stable Gain (V/V)	+1	+1	+5	±2	±10
Settling Time (ns, to 0.1%)	140	110	90	180	200
Shutdown Time (ns)	400	400	400	400	NA
Supply Current (mA)	32	32	32	37	37
Gain Error (%)	NA	NA	NA	0.1	0.5

LT1190 continued from page 11

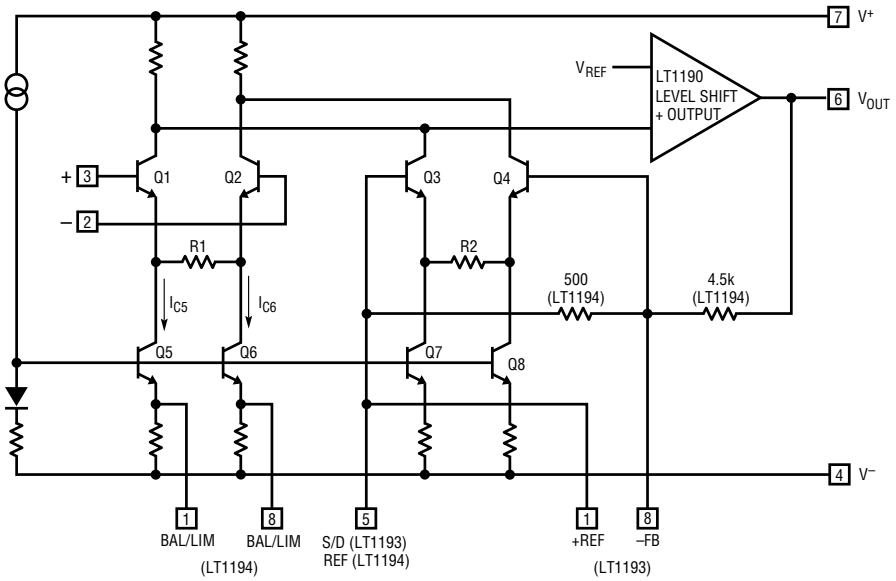

Figure 3. The LT1194 has Adjustable Input Limiting Through the Balance Pins and Fixed Gain. The LT1193 has Shutdown Capability and User-Defined Gain

and the balance pins are externally available at pins 1–8. Pins 1 and 8 can optionally be used for either conventional DC-offset balancing, or for input limiting to prevent overload.

For use as a current mode limiter, the LT1194 input stage operates as follows: The maximum allowable input signal is determined by the maximum available current swing in R1. This is set for an input condition which tilts the differential input stage completely to one side, allowing either Ic5 or Ic6 to develop voltage across R1. By externally shorting the balance pins together and raising them above the V– rail, the currents in Q5 and Q6 are reduced, lowering the maximum drop across R1, and thereby lowering the maximum input signal. Figure 4 demonstrates the effect of the limiting voltage on the maximum output voltage.

Since no devices saturate in this limiting process, the result is very fast and clean limiting, with the exact level user controllable. When Q1, Q2, Q5, and Q6 are completely turned off, the output-level, DC-loop integrity is maintained through the feedback path of Q3-Q4.

Applications

The video loop-through connection is a popular method of connecting different pieces of equipment. Prior to its widespread use, the usual method of connection was the video distribution box, a "fan-out" method of signal distribution. Although limited in flexibility, this method did provide proper cable termination. In contrast, the loop-through connection distributes signals by a daisy chain approach, passing the signal continuously to each subsequent piece of equipment, with the last site providing cable termination. At each tap along the loop, the signal is locally replicated by an amplifier, with minimal disturbance to the line.

Each tap location requires a video differential amplifier with good CMRR at high frequency. This is necessary because there are ground loops between pieces of equipment, and high frequency common mode noise is often induced in the cable.

While a fast op amp and a well-matched resistor network can make such a differential amplifier, performance suffers with all but video-rated op amps, such as the LT1191/92/93. A pair of current-feedback amplifiers, such as LT1223s[1] can also be used to make a differential amplifier, but at a cost of two ICs plus the resistor network. In studio NTSC applications, where the high voltage swings of the LT1223 are not absolutely required, a single video-difference IC is more efficient, as well as more cost-effective.

Figure 5 shows the LT1193 used in a unity-gain, loop-through connection, with a -3dB bandwidth of 80MHz. The signal is distributed to each subsequent site, and the LT1193 is configured by R_F and R_G for a gain of 2, since back termination of the cable attenuates the signal by 6 dB. R_T is the termination resistor, with the output

continued on page 15

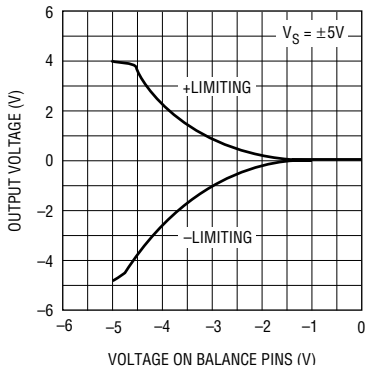

Figure 4. LT1194 Maximum Output Voltage vs Voltage on Balance Pins

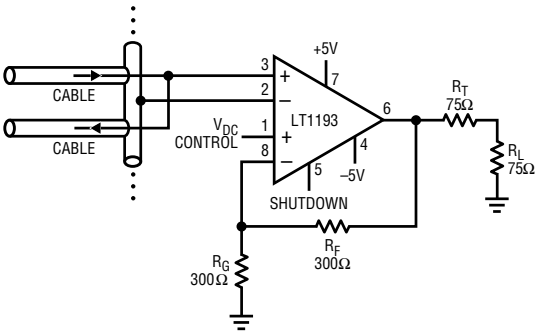

Figure 5. Video Loop Through Connection with DC Control, –3dB Bandwidth is 80MHz

LTC1264-7 continued from page 4

transmission of f_s symbols in a bandwidth (bw=B) of only $f_s/2$ Hertz. For a binary transmission, where one symbol contains one bit, f_b, the number of bits-per-second is equal to the symbol rate, f_s. For "*M*-ary" systems, such as four-level pulse amplitude modulation (PAM), each transmitted symbol contains *n* information bits, where $n = \log_2 M$. In this case, the symbol rate is $f_s = f_b/n$. Consider the example where it is required to transmit a 100Kb/sec. source ($=f_b$). Theoretically, this could be accomplished with a channel bandwidth $B = f_s/2 = f_b/2 = 50kHz$. With the above mentioned four-level PAM scheme the channel bandwidth is reduced to $25kHz = f_s/2 = f_b/4$.

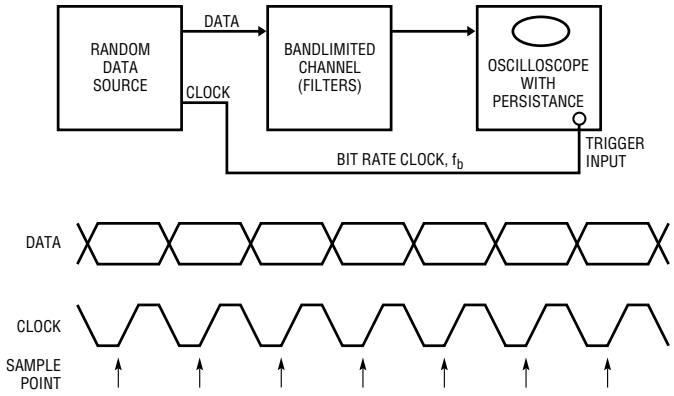

Figure 3. Eye Diagram Generation Circuitry and Data Timing

The Eye Diagram

Since the perfect, low-passed transmission channel does not exist, a means must be found to evaluate channel quality. The means is the so called "eye" diagram. The eye diagram is generated by the setup shown in Figure 3.

Symbols transmitted through a theoretical channel (Nyquist) have no degradation in amplitude response, and hence the measured eye diagram opening of a real channel shows graphically the "quality" of the transmission channel, which includes the low-pass filter inserted in the transmission path. It can be shown that the degradation in the eye opening is directly related to inter-symbol interference (the interference in the detection of one symbol in the presence of another), and therefore is a measure of the system's bit-error rate. (see Feher)[1]

With this background, let's look at some "eye opening" diagrams to see how we have optimized the LTC1264-7 filter for applications in data communications.

Figures 4 and 5 show the eye diagrams of the LTC1064-2 (eighth-order Butterworth LPF) and the new LTC1264-7 linear-phase filter (sixth-order elliptic LPF plus second-order, phase correction network). It can be seen that if a digital system switches at the midpoint in the eye diagrams, the bit-error rate (BER) will be higher for the eye diagram with the smaller "eye opening." The calculation of inter-symbol interference degradation due to channel or filter imperfections is a measure of degradation in BER and is calculated:

ISI degradation = 20 log (actual eye opening/100% eye opening)

Thus, it can be seen that the LTC1264-7 is a far superior filter when used to maximize channel efficiency in a digital system. However, we still need to look at the LTC1064-3 (eighth-order Bessel LPF) for comparison.

Figure 6 is the eye diagram of the LTC1064-3. This

continued on page 15

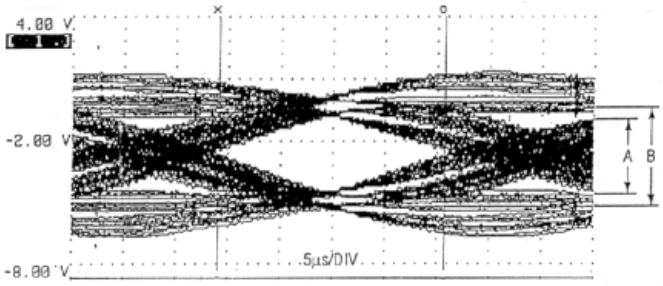

Figure 4. LTC1064-2: f_{CUTOFF} = 13.7kHz, f_S = 27.5kb/s. ISI Degradation = 20 Log (0.75) = –2.5dB. A = 75% Opening, B = 100% Opening.

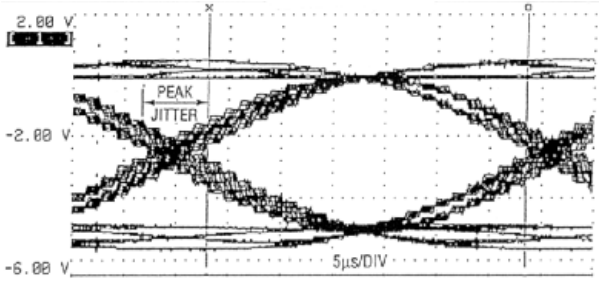

Figure 5. LTC1264-7: f_{CUTOFF} = 13.7kHz, f_S = 27.5kb/s. ISI Degradation = –0.46dB, Peak Jitter = ~5.6µs.

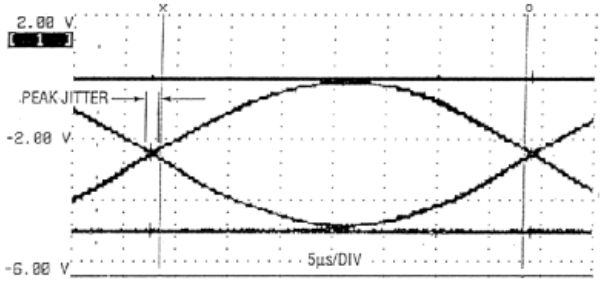

Figure 6. LTC1064-3: f_{CUTOFF} = 13.7kHz, f_S = 27.5kb/s. ISI Degradation = –0.94dB, Peak Jitter = ~1.2µs.

LTC1100 continued from page 5

and LT1102. The 8-pin LTC1100 has a fixed gain of 100, but makes the summing points available for user connections. The key specifications of these three devices are summarized in Table 1.

It is apparent from Table 1 that for these three IA's, there are no output contributions to input errors. With dedicated IA's or with the three-op-amp configuration, there are separate specifications for input and output offset voltage, input and output drift and noise, and input and output power-supply rejection ratio. To calculate system errors, these input and output terms must be combined. With the 1100/01/02, these error calculations are simple.

With these three IA choices, the user can optimize performance for a variety of factors. The LTC1100 operates with dual or single supplies ranging from 4V to 18V, whereas the LTC1101 accepts a supply range of from 1.8V to 40V. In addition, the LT1101 consumes only 100µA standby current. For applications that require very low offset voltage and drift, the LTC1100 excels, with 1µV of offset and 5nV/°C drift. Where both high speed and low bias current are important, the LT1102 is the IA of choice, albeit at a cost of slightly higher power consumption and dual supplies. As can be seen from the table, all of these devices are outstanding with regard to gain accuracy, linearity and stability. The LTC1100, which is based on a dual-chopper amplifier prototype (the LTC1051), is by far the best in terms of offset and drift. Either the LTC1100 or the LT1102 could be the unit of choice in terms of lowest bias current, with the LT1102 gaining an edge at higher temperatures.

Application Considerations

While this IA type is generally outstanding in terms of performance and simplicity, independent of the op amps, some caveats apply to using it most effectively. One concern is AC CMRR. As noted in Figure 2, the first op amp (A) is configured for unity gain, while the second op amp (B) provides all of the voltage gain. This has the effect of making the respective CMRR's frequency mismatched, since the CMRR of the higher-gain, "B" side corners at a much lower frequency. The resulting differential CMRR will therefore degrade more quickly with frequency than that of a topology with better AC balance. On the LT1102 this problem is resolved by decompensating amplifier B to gain-often stability. This increases slew rate and bandwidth, and also matches the CMRR roll-off with the frequencies of the two op amps when G = 10. At a gain of 100, this roll-off match no longer holds. However, connecting an 18pF capacitor between pins 1 and 2 matches the CMRRs of the two sides and improves CMRR by an order of magnitude in the 300Hz-30kHz range (Figure 3). As shown on the LTC1100 and 1101 data sheets, similar improvements can be obtained from those devices by connecting external capacitors.

Table 1. LTC Instrumentation Amplifier Specifications[1]

	LTC1100C	LT1101M/I/C	LT1102M/I/C
Available gains	100[2]	10/100	10/100
Gain error (%)	0.01	0.01	0.01
Gain non-linearity (ppm)	3	3	7
Gain drift (ppm/°C)	2	2	10
V_{os} (µV)	1	60	200
V_{os} drift(µV/°C)	0.005	0.5	3
I_b (pA)	2.5	6000	4
I_{os} (pA)	10	150	4
e_n	1.9µVp–p (DC–10Hz)	0.9µVp–p (0.1–10Hz)	20nV/(Hz)$^{1/2}$ (@1kHz)
CMRR (dB)	110	112	98
PSRR (dB)	130	114	102
Vs (total, mode)	4–18V (single/dual)	1.8–44V (single/dual)	10–44V (dual)
Is (mA)	2.4	0.09	3.4
Gain-bandwidth (MHz)	2	0.37	35
SR (V/µs)	4	0.1	30

[1] Unless otherwise stated, all specs are typical at Ta=25°C. Vs=±15V for LT1101/LT1102, and ±5V for LTC1100.
[2] A gain option of 10/100 is available in LTC1100CS (16-pin SOL).

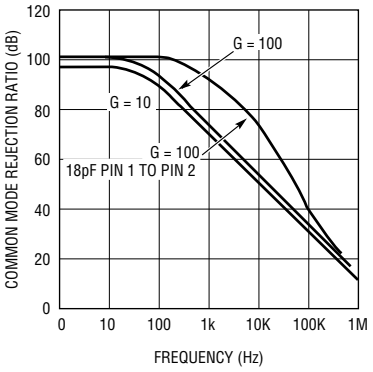

Figure 3. LT1102 Common-Mode Rejection Ratio vs Frequency

The LTC1100 and LT1101 also present some important usage considerations because of their single-supply abilities, i.e., when operating with the V– terminal tied to ground. In this configuration, these devices handle CM inputs near ground and voltage

continued on page 15

LTC1155
continued from page 7

control the MOSFET gate voltage and maintain a constant 5V at the output.

The regulator is switched ON and OFF by the control logic or the microprocessor to conserve power in the standby mode. The LTC1155 standby current drops to about 10µA when the input is switched OFF. The total ON current, including the LT1431, is less than 1mA.

LT1190
continued from page 12

appearing across load resistor R_L. Use of the shutdown pin is optional, and the output DC level can be adjusted if desired, by a voltage applied to the V_{DC} input. When this pin is grounded, the output is centered at 0 volts.

The low-cost LT1190 family of op amps and video difference amps will find its way into many applications, including I/V converters, fast integrators, active filters, and photo-diode amplifiers, in addition to tape and disc drive products and instrumentation.

[1] See Bill Gross' "The LT1223, a New High Speed Current Feedback Amplifier," *Linear Technology*, Volume 1, Number 1, June 1991.

LTC1264-7
continued from page 13

diagram shows ISI degradation similar to that of the LTC1264-7, with better jitter specifications. Although the Bessel filter appears to be superior from the viewpoint of the eye diagram, the reader should remember that the LTC1264-7 has far superior stopband attenuation, meaning better attenuation of the carrier (at 27.5kHz in this example). This translates to better bit-error rates. The system user must trade off ISI degradation, jitter, and stopband attenuation to ensure the best channel performance. In addition, remember that the eye diagrams shown here are for two-level systems (0 and 5 volts). For M-level systems, the increasedspectrum efficiency means greatersignal-to-noise ratios are required,necessitating the rolloff characteristics of filters like the LTC1264-7.

To conclude, the LTC1264-7 is a linear-phase, "better than Bessel," switched-capacitor filter, optimized for data communications applications. The filter will operate to a cutoff frequency of 200kHz while providing linear phase through its passband. The filter can be used in satellite communications, cellular phones, microwave links, ISDN networks and many other types of digital systems.

References:

1. Feher, Kamilo. *Digital Communications: Microwave Applications.* Englewood Cliffs, New Jersey: Prentice-Hall Inc., 1981
2. Feher, Kamilo, and Engineers of Hewlett Packard Ltd. *Telecommunications, Measurements, Analysis and Instrumentation.* Englewood Cliffs, New Jersey: Prentice-Hall, Inc., 1987
3. Feher, Kamilo. *Digital Communications: Satellite/Earth Station Engineering.* Englewood Cliffs, New Jersey: Prentice-Hall, Inc., 1981

LT1100, LT1101 and LT1102
continued from page 14

swings to ground, and their reference terminals can be tied to ground. One of the most common uses of these two IA's is as bridge amplifiers, in conjunction with single-supply-powered DC strain gauges. As such, these IA's have a unique ability to deliver high gain with precision, while operating with a 1/2-supply-voltage CM input. At first glance, it appears that a dual-supply IA could operate, for example, on a 9V battery supply, with 4.5V common-mode input, but its output will not swing to ground, and its reference terminal cannot be tied to ground.

For SPICE simulation purposes, a model for the LT1101 is included in the LTC macromodel library. The model is configured as the resistor network shown for the LT1101, combined with a model for the LT1078. A similar model for the LTC1100 can be made by scaling the four resistors appropriately, and using an LTC1051 model from the same library. A close model approximation for the LT1102 can be made with the LT1102 resistor values, combined with an LT1057 model for the "A" side, and a LT1022 model for the "B" side (both also in the library).

High Frequency Op Amp Design Hints

High speed operational amplifier design is a non-trivial task which requires careful layout, attention to stray capacitance, separation of input and output grounds and other techniques which the casual designer of low frequency circuits is not familiar with.

Linear Technology now has two publications which deal specifically with the difficulties of designing with high speed operational amplifiers.

Application Note 47, an opus by Jim Williams entitled "High Speed Amplifier Techniques" contains numerous segments detailing problems encountered in high speed circuit design. In addition to a section entitled "Perspectives on High Speed Design" there is a section entitled "Mr. Murphy's Gallery of High Speed Amplifier Problems." Williams also includes a tutorial section which discusses cables, probes, ground planes and other techniques which are essential to the proper design and characterization of high speed circuitry. Applications are, of course, also included in profusion on a variety of topics including amplifiers, oscillators, and data conversion. Application Note 47 is available upon request from Linear Technology Corp.

Design Note 50 by Mitchell Lee describes a High Frequency Amplifier Evaluation Board which is available from LTC. Mitchell, in this Note, summarizes many of the techniques which Williams describes in detail. A demonstration circuit layout is also available for use in layout and/or breadboarding of prototype circuitry. Design Note 50 is available upon request from LTC.

LT1109 Generates V_{pp} for Flash Memory

by Steve Pietkiewicz

Flash memory chips such as the Intel 28F020 2Megabit device require a V_{pp} program supply of 12 volts at 30mA. A DC–DC converter may be used to generate 12 volts from the 5 volt logic supply. The converter must be physically small, available in surface-mount packaging, and have logic-controlled shutdown. Additionally, the converter must have carefully controlled rise time and zero overshoot. V_{pp} excursions beyond 14 volts for 20ns or longer will destroy the ETOX[1]-process based device.

Figure 1's circuit is well suited for providing V_{pp} power for a single flash memory chip. All associated components, including the inductor, are surface mount devices. The $\overline{\text{SHUTDOWN}}$ input turns off the converter, reducing quiescent current to 300µA when pulled to a logic 0. V_{pp} rises in a controlled fashion, reaching 12 volts ±5% in under 4ms. Output voltage goes to V_{cc} minus a diode drop when the converter is in shutdown mode. This is an acceptable condition for Intel flash memories and does not harm the memory.

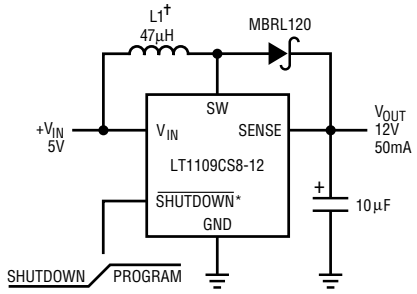

Figure 1. All Surface Mount Flash Memory Vpp Generator

[1]ETOX is a trademark of Intel Corporation.

RF Leveling Loop

by Jim Williams

Leveling loops are often a requirement for RF transmission systems. More often than not, low cost is more important than absolute accuracy. Figure 1 shows such a circuit.

The RF input is applied to A1, an LT1228 operational transconductance amplifier. A1's output feeds A2, the LT1228's current-feedback amplifier. A2's output, the output of the circuit, is sampled by the A3-based gain control configuration. This arrangement closes a gain-control loop back at A1. The 4pF capacitor compensates rectifier diode capacitance, enhancing output flatness vs frequency. A1's I_{SET} input current controls its gain, allowing overall output level control. This approach to RF leveling is simple and inexpensive, and provides low output drift and distortion.

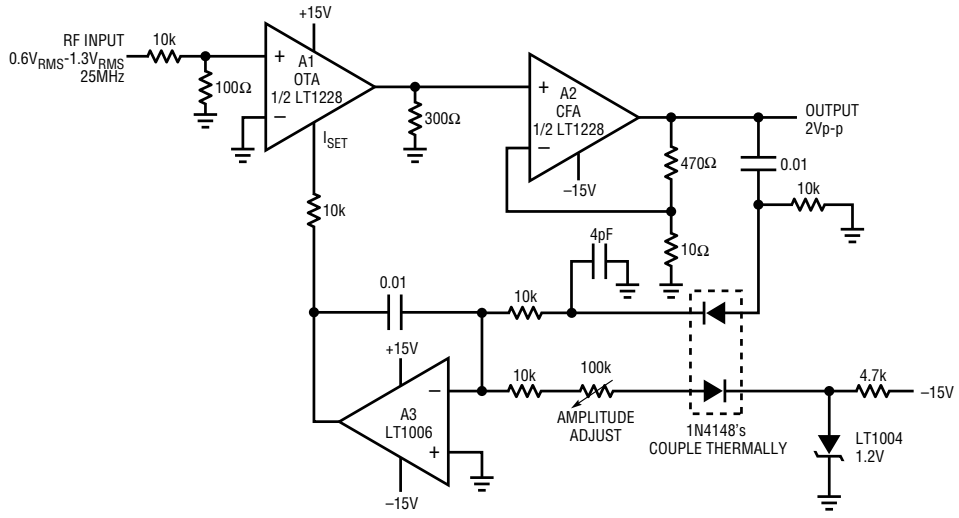

Figure 1. Simple RF Leveling Loop

Ultra-low Noise and Low Drift Chopped-FET Amplifier

by Jim Williams

Figure 1's circuit combines the extremely low drift of a chopper-stabilized amplifier with a pair of low noise FETs. The result is an amplifier with 0.05µV/°C drift, offset within 5µV, 100pA bias current and 50nV noise in a 0.1Hz–10Hz bandwidth. The noise performance is especially noteworthy; it is almost 35 times better than monolithic chopper-stabilized amplifiers.

FETs Q1 and Q2 differentially feed A2 to form a simple low-noise op amp. Feedback, provided by R1 and R2, sets closed-loop gain (in this case 10,000) in the usual fashion. Although Q1 and Q2 have extraordinarily low noise characteristics, their offset and drift are uncontrolled. A1, a chopper-stabilized amplifier, corrects these deficiencies. It does this by measuring the difference between the amplifier's inputs and adjusting Q1's channel current via Q3 to minimize the difference. Q1's skewed drain values ensure that A1 will be able to capture the offset. A1 and Q3 supply whatever current is required to force offset to within 5µV into Q1's channel. Additionally, A1's low bias current does not appreciably add to the overall 100pA amplifier bias current. As shown, the amplifier is set up for a non-inverting gain of 10,000, although other gains and inverting operation are possible. Figure 2 is a plot of the measured noise performance.

The FETs' Vgs can vary over a 4:1 range. Because of this, they must be selected for 10% Vgs matching. This matching allows A1 to capture the offset without introducing any significant noise.

Figure 3 shows the response (trace B) to a 1mV input step (trace A). The output is clean, with no overshoots or uncontrolled components. If A2 is replaced with a faster device (e.g. LT1055) speed increases by an order of magnitude with similar damping. A2's optional overcompensation can be used (capacitor to ground) to optimize response for low closed loop gains.

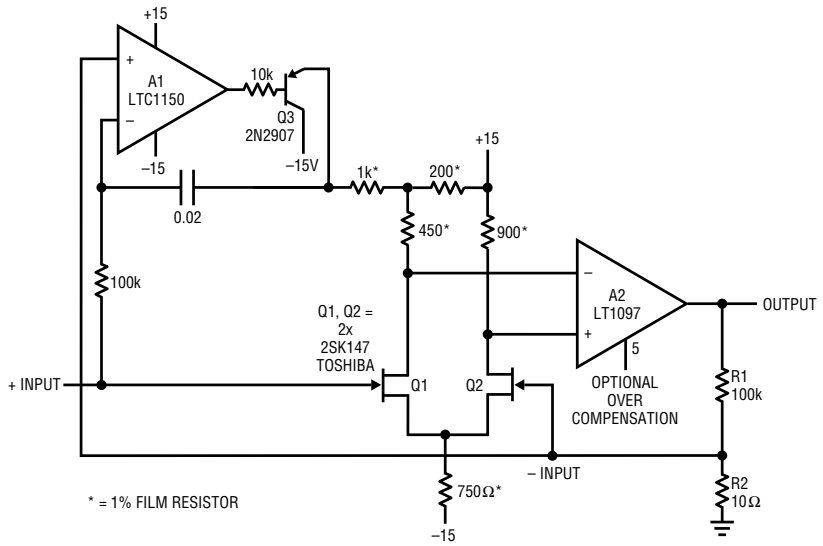

Figure 1. Chopper Stabilized FET Pair Combines Low Bias, Offset and Drift with 45nV Noise

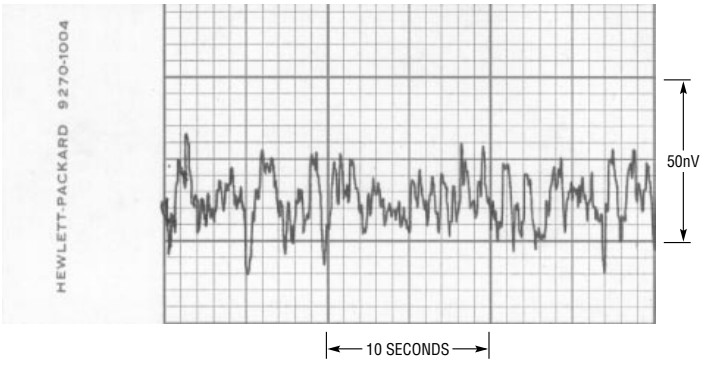

Figure 2. 45nV Noise Performance for Figure 1. A1's Low Offset and Drift are Retained, but Noise is Almost 35 Times Better

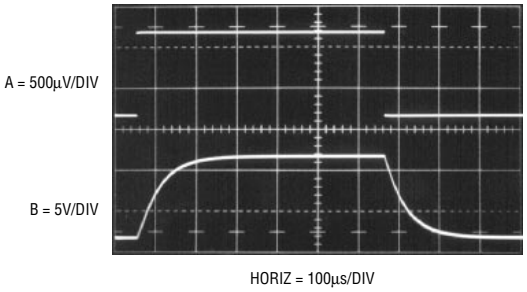

Figure 3. Step Response for the Low Noise +10,000 Amplifier. A 10x Speed Increase is Obtainable by Replacing A2 with a Faster Device

New Device Cameos

by LTC Marketing

LT1027 High-Accuracy 5V Reference

The LT1027 is the industry's most precise 5V reference. The LT1027C grade provides 0.05% maximum initial accuracy and 3 ppm/°C maximum output-voltage drift with temperature. The LT1027D grade has 0.05% maximum initial accuracy, with 5 ppm/°C maximum temperature drift. The LT1027E grade provides 0.1% maximum initial accuracy, and 7.5 ppm/C° maximum temperature drift. All three grades improve upon the industry-standard precision 5V reference, the LT1021-5. This high level of performance is obtained without the use of a power-hungry heated substrate.

In addition to excellent accuracy and drift performance, the LT1027 provides 2µs settling to 0.01%. Settling time can be improved to 500ns by connecting a 4.7µF tantalum capacitor between VOUT and ground.

The LT1027 reference voltage is derived from a buried-zener reference, which provides excellent low-noise characteristics (10Hz to 1kHz noise is 2µV RMS) and excellent long-term stability (20 ppm/month for the TO-5 package). Connecting a 1µF capacitor between the noise reduction (NR) pin and ground reduces 10Hz to 1kHz noise to 1.2µV RMS. The LT1027 guarantees a ±30mV trim range with a 10k trimpot. Unlike previous references, trimming doesn't affect the temperature coefficient of the device.

LT1082 1A High-Voltage, High-Efficiency Switching Regulator

The LT1082 is a 60kHz switching voltage regulator, designed for high-voltage, low-current applications such as isolated and non-isolated –48V to 5V telecom supplies. All control circuitry and a high-efficiency 1A power switch are included in a compact 8-pin minidip, 5-lead TO-220, or 5-lead TO-3 package. The LT1082 utilizes current-mode switching techniques to obtain excellent AC and DC line and load regulation. The LT1082 operates in all standard switching topologies. In the isolated-flyback mode the LT1082 senses the primary-flyback voltage to regulate output voltage, without the need of an optoisolator.

The LT1082 can provide 5V at 800mA from –48V, while consuming only 4.5mA quiescent current. The LT1082 features a high maximum-input voltage of 75V and a maximum switch voltage of 100V, making it ideal for isolated and non-isolated –48V to +5V converters. The LT1082 can easily be shutdown to 120µA supply current. When the output is shorted, the LT1082 lowers its operating frequency from 60kHz to 16kHz to protect the outputs, even with 70 volts at the input.

LT1124, LT1126 Dual and LT1125, LT1127 Quad Low-Noise Op Amps

Linear Technology's new LT1124 dual and LT1125 quad low-noise, high-speed, precision operational amplifiers outperform the industry standard OP27 single op amp as well as the OP270 dual and OP470 quad op amps they are designed to replace. The individual amplifiers in each LT1124 and LT1125 are 100% tested for input voltage noise (4.2 nV/root Hz maximum), something that has not been done with their predecessors. The LT1124 is the first low-noise, high-speed, precision dual op amp to be offered in the 8-pin, small-outline surface-mount package.

Usually, dual and quad performance is inferior to that of single op amps due to the difficulty of designing and manufacturing multiple op amps. In this case the performance is better. The LT1124 and LT1125 have faster slew rate and greater bandwidth, lower bias and offset currents, and higher gain than the OP27. The total supply current of the dual LT1124 is less than the supply current of the OP27 single. The LT1124 and LT1125 have lower offset voltage and bias current and higher slew rate, bandwidth, and gain than the OP270 and OP470 devices Comparable specifications are improved by a factor of two, not just a few percent.

Decompensated versions of these devices are also available. The LT1126 dual and LT1127 quad are stable in closed-loop gains of ten or more. The slew rate of the LT1126/27 is 2.5 times faster and the gain-bandwidth product is four times higher than those of the LT1124/25. Thus, the LT1126/27 can upgrade systems using the decompensated OP37 single op amp.

LT1228 100MHz Current Feedback Amplifier with DC Gain Control

The LT1228 is the first monolithic video amplifier with electronic gain control. The 8-pin packaged LT1228 uses a 75MHz transconductance amplifier and 100MHz current feedback amplifier to realize AGC amplifiers, tunable filters, sinewave oscillators, audio and video mixers, audio and video faders, and DC restore circuits. A differential input, DC gain controlled amplifier is easily made with the LT1228 and just a few resistors. Now it is possible to locate gain trim pots at the front of professional video equipment without having to route the video signals all over the PC board.

The variable gain transconductance amplifier is the heart of the LT1228 and it has over a 60dB of gain control range. The output of the transconductance amplifier is buffered by the built in current feedback amplifier for an output drive current capability of 30mA. The current feedback amplifier is optimized for video performance; when driving a cable, the differential gain is only 0.04% and the differential phase is 0.10 degrees. When driving an A to D converter these specs improve to 0.01% and 0.01 degrees!

These features and the wide supply range of ± 2V (4V total) to ±15V (30V total) make it easy to use the LT1228 in almost any system.

In RGB and other computer video systems, the excellent transient response of the current feedback amplifier eliminates smearing (rise time is only 3.5ns). The DC control to the LT1228 is a current to simplify the interfacing of remotely located control circuitry.

The LT1228 is available in 8-pin dual-in-line plastic and ceramic packages as well as the 8-pin small outline packages. Military, industrial and commercial temperature range versions are available.

LTC1046 50mA Switched-Capacitor Voltage Converter

Our newest switched-capacitor voltage converter, the LTC1046, is designed for voltage inversion and doubling in 3–6V battery-powered systems, where voltage loss and quiescent current are critical. The LTC1046's output resistance of only 35Ω maximum translates to a 65% reduction in voltage loss compared to the LTC1044 and ICL7660. The LTC1046 does this while consuming only 300µA maximum supply current. The LTC1046 provides a power-conversion efficiency of 97% and a voltage-conversion efficiency of 99.9% (no load). Oscillator frequency is nominally 30kHz when operating on a 5V supply, and can be increased with use of a boost pin to optimize efficiency for a particular application. The LTC1046 is functionally and pin-for-pin compatible with the LTC1044 and the ICL7660, but provides 2.5 times the drive capability for 6V and lower voltage conversion applications.

LTC1164-5 8th-Order Butterworth or Bessel and LTC1164-6 8th-Order Elliptic Low Pass Filters

The LTC1164-5 and LTC1164-6 offer the user low supply currents (4mA with ±5V supplies), low wide-band noise (100µV RMS for the LTC1164-5 and 120µV RMS for the LTC1164-6), and low THD (less than 0.02%) in a compact 14-pin package. No external resistors are required to realize the filter functions. Cutoff frequencies up to 20kHz (±7.5V supplies) or up to 10kHz (±5V supplies) can be achieved.

The LTC1164-5 can be configured either as an 8th-order Butterworth (100:1 or 50:1 clock to cutoff frequency ratio), or as an 8th-order Bessel (150:1 clock ratio) low pass filter. The LTC1164-6 is an 8th-order elliptic low pass filter with 64dB attenuation at 1.45 times the cutoff frequency at a 100:1 clock to cutoff frequency ratio. Both the LTC1164-5 and the -6 can operate on a single 5V supply with a 1V RMS input signal. Typical applications for the LTC1164-5 and LTC1164-6 include low-power data-acquisition systems, battery-powered instruments, and telecommunications.

CMOS RS485 Interface Family

LTC's growing family of RS485 interface devices now includes seven members that are compatible with industry-standard pinouts and achieve significant power savings. The first member, the LTC485 half-duplex transceiver, reduces power consumption by 60X when dropped into 75176 sockets, for applications up to 2.5MHz. The LTC486 and LTC487 quad-differential line drivers draw only 200µA maximum supply current, and directly replace the 75172 and 75174 quad drivers for applications up to 10MHz. Their companion differential line receivers, the LTC488 and LTC489, drop into 75173 and 75175 sockets to obtain a 10X power reduction and data rates up to 10MHz. For full-duplex, 4-wire RS485 interface applications, LTC offers the LTC490 and LTC491 full-duplex transceivers which directly replace the 75179 and 75ALS180 transceivers with at least a 60X power savings. The LTC490 and LTC491 support data rates up to 5MHz. All LTC CMOS RS485 line drivers drive cables of up to 4000 feet at slower data rates.

All members of the LTC CMOS RS485 family utilize a unique fabrication process and design that places Schottkey diodes in series with the MOS output transistors, to maintain a high impedance state when the outputs are forced up to 7V beyond the supply rails or when the device is off. This crucial RS485 specification allows for a ±7V common-mode voltage between drivers on an interface line. Output-current limit and full thermal-overload protection are incorporated on all LTC RS485 products. The full line is offered in DIP and surface-mount packages for use over the commercial and industrial temperature ranges.

LT1229/30 Dual and Quad Current-Feedback Amplifiers

The LT1229 is a dual current-feedback amplifier that provides 100MHz bandwidth, 1000V/µs slew rate, and 30mA minimum output drive capability, in a space-saving 8-lead DIP or 8-lead SOIC package. The LT1229 settles to 0.1% in 45ns and draws 6mA supply current per amplifier. The LT1229 operates on supplies ranging from ±2V to ±15V with an input-voltage range and output swing to within 1.5V of the supply rails. The LT1230 quad offers the same performance as the LT1229 in a 14-pin DIP or 14-pin SOIC package. Both the LT1229 and LT1230 are optimized for video performance. The differential gain and phase are only 0.04% and 0.1 degrees when driving a 75Ω cable and drop to 0.01% and 0.01 degrees when driving flash A to D converters.

The LT1229's and LT1230's 25MΩ input impedance and 30mA minimum output drive make the devices useful as buffers and video instrumentation amplifiers, and excellent for general high-speed cable-driving applications.

For further information on the above or any other devices mentioned in this issue of Linear Technology, use the reader service card or call the LTC literature service number, (800) 637-5545. Ask for the pertinent data sheets and application notes.

DESIGN TOOLS

Applications on Disk

NOISE DISK
This IBM-PC (or compatible) progam allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise, and calculate noise using specs for any op amp.

SPICE MACROMODEL DISK
This IBM-PC (or compatible) high density diskette contains the library of LTC op amp SPICE macromodels. The models can be used with any version of SPICE for general analog circuit simulations. The diskette also contains working circuit examples using the models, and a demonstration copy of PSPICE™ by MicroSim.

FILTERCAD DISK
FilterCAD is a menu-driven filter design aid program which runs on IBM-PCs (or compatibles). This collection of design tools will assist in the selection, design, and implementation of the right switched capacitor filter circuit for the application at hand. Standard classical filter responses (Butterworth, Cauer, Chebyshev, etc.) are available, along with a CUSTOM mode for more esoteric filter responses. SAVE and LOAD utilities are used to allow quick performance comparisons of competing design solutions. GRAPH mode, with a ZOOM function, shows overall or fine detail filter response. Optimization routines adapt filter designs for best noise performances or lowest distortion. A design time clock even helps keep track of on-line hours.

Technical Books

Linear Databook — This 1,600 page collection of data sheets covers op amps, voltage regulators, references, comparators, filters, PWMs, data conversion and interface products (bipolar and CMOS), in both commercial and military grades. The catalog features well over 300 devices. $10.00

Linear Applications Handbook — 928 pages chock full of application ideas covered in-depth through 40 Application Notes and 33 Design Notes. This catalog covers a broad range of "real world" linear circuitry. In addition to detailed, systems-oriented circuits, this handbook contains broad tutorial content together with liberal use of schematics and scope photography. A special feature in this edition includes a 22-page section on SPICE macromodels. $20.00

Monolithic Filter Handbook — This 232 page book comes with a disk which runs on PCs. Together, the book and disk assist in the selection, design and implementation of the right switched capacitor filter circuit. The disk contains standard filter responses as well as a custom mode. The handbook contains over 20 data sheets, Design Notes and Application Notes. $40.00

World Headquarters

Linear Technology Corporation
1630 McCarthy Boulevard
Milpitas, CA 95035-7487
Phone: (408) 432-1900
FAX: (408) 434-0507
Telex: 499-3977

U.S. Area Sales Offices

NORTHEAST REGION
Linear Technology Corporation
One Oxford Valley
2300 E. Lincoln Hwy. Suite 306
Langhorne, PA 19047
Phone: (215) 757-8578
FAX: (215) 757-5631

SOUTHEAST REGION
Linear Technology Corporation
3442 E. Lake Road
Suite 314
Palm Harbor, FL 34685
Phone: (813) 784-0244
FAX: (813) 787-5853

CENTRAL REGION
Linear Technology Corporation
415 West Golf Road
Suite #24
Arlington Heights, IL 60005
Phone: (708) 228-6999
FAX: (708) 228-7013

SOUTHWEST REGION
Linear Technology Corporation
22141 Ventura Boulevard
Suite 206
Woodland Hills, CA 91364
Phone: (818) 703-0835
FAX: (818) 703-0517

NORTHWEST REGION
Linear Technology Corporation
1630 McCarthy Boulevard
Milpitas, CA 95035-7487
Phone: (408) 432-1900
FAX: (408) 434-0507

International Sales Offices

FRANCE
Linear Technology S.A.R.L.
143 Grande Rue
92310 Sevres
France
Phone: 33-1-45341210
FAX: 33-1-45341548

JAPAN
Linear Technology KK
4F Ichihashi Building
1-8-4 Kudankita Chiyoda-Ku
Tokyo, 102 Japan
Phone: 81-3-237-7891
Telex: 33801
FAX: 81-3-237-8010

KOREA
Linear Technology Korea Branch
Namsong Building, #505
Itaewon-Dong 260-199
Yongsan-Ku, Seoul
Korea
Phone: 82-2-792-1617
FAX: 82-2-792-1619

SINGAPORE
Linear Technology PTE. LTD.
101 Boon Keng Road
#02-15 Kallang Ind. Estates
Singapore 1233
Phone: 65-293-5322
FAX: 65-292-0398

TAIWAN
Linear Technology Corporation
Rm. 801, No. 46, Sec. 2
Chung Shan N. Rd.
Taipei, Taiwan, R.O.C.
Phone: 886-2-521-7575
FAX: 886-2-521-7575

UNITED KINGDOM
Linear Technology (UK) Ltd.
111, Windmill Road
Sunbury, Middlesex TW16 7EF
United Kingdom
Phone: 44-932-765688
Telex: 883101
FAX: 44-932-781936

GERMANY
Linear Technology GMBH
Untere Hauptstr. 9
D-8057 Eching
Germany
Phone: 49-89-3197410
Telex: 17-897457
FAX: 49-89-3194821

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Boulevard
Milpitas, CA 95035-7487
(800) 637-5545

LINEAR TECHNOLOGY